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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,819	06/27/2003	Rajesh Kota	NWISP046	8385

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EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	**PAPER NUMBER**
2153	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,819	KOTA ET AL.	
	Examiner	Art Unit	
	LaShanya R. Nash	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the amendment filed 29 May 2007. Claims 1-31 are presented for further consideration. Claims 1-31 are as originally presented.

Response to Arguments

Applicant's arguments, see Remarks, filed 29 May 2007, with respect to the rejections of claim 1 under §102(b) and claims 2-31 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of newly found references Self et al. (US Patent 5,623,644), Booth (US Patent 6,065,073) and Kelly et al. (US Patent 5,379,440), as set forth below in the Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view of Booth (US Patent 6,065,073), hereinafter referred to as Self and Booth.

In reference to claim 1, Self discloses a point-to-point communication apparatus (abstract). Self further discloses:

- A computer system (Figures 17-18), comprising:
- A first cluster (i.e. micro-cluster; Figure 18-item 1850; column 14, lines 1-14) including a first plurality of processors (Figure 18-items 1812-1813) and a first interconnection controller (i.e. router/memory controller; Figure 18-item 1811), the first plurality of processors and the first interconnection controller in communication using a point-to-point architecture (i.e. point-to-point interconnection; column 10, lines 35-52; column 14, lines 10-14);
- A second cluster (Figure 18-item 1851) including a second plurality of processors (Figure 18-processors for cluster 1851) and a second interconnection controller (Figure 18-router/memory controller), the second plurality of processors and the second interconnection controller in communication using a point-to-point architecture (column 10, lines 35-52; column 14, lines 10-26).

However, the reference fails to teach wherein polling for a link from the first interconnection controller to the second interconnection controller can be enabled or disabled by configuring the first interconnection controller. Nonetheless, enabling and disabling polling was a well-known feature in the art, at the time of the invention, as further evidenced by Booth. Therefore, it would have been obvious for one of ordinary skill in the art to accordingly modify the features of Self.

In an analogous art, Booth discloses polling for network link (abstract). Booth further discloses wherein polling for a link can be enabled or disabled by configuring the first interconnection controller (column 20, line 55-column 21, line 6). One of ordinary skill in the art at the time of the invention, would be motivated to according modify the system of Self with enabled/disabled polling so as to provide link monitoring for establishing communication links, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40).

In reference to claim 2, Self shows the first cluster of processors and the second clusters of processors share a single virtual address space (column 11, lines 46-column 12, line 8).

In reference to claim 3, Booth shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8).

In reference to claim 4, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim 5, Self shows wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 6. Self shows wherein reinitialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 7, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claim 8, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

In reference to claim 9, Self shows wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 10, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 11, Self shows wherein the first interconnection controller includes, fence, reinitialization and cluster ID bits (column 11, lines 46-column 12, line 8; column 11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Claims 12-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view of and Kelly et al. (US Patent

5,379,440) and Booth (US Patent 6,065,073), hereinafter referred to as Self and Kelly and Booth.

In reference to claim 12 and 23, Self discloses a point-to-point communication method and point-to-point apparatus communication (abstract), Self further discloses:

- A method for introducing a cluster of processors the method comprising:
    - Configuring a first interconnection controller (i.e. memory controller/router; Figure 18-item 1811) in a first cluster (Figure 1-item 1730) including a first plurality of processors (Figure 17-items 1711,1713) in communication using a point-to-point architecture (i.e. point-to-point interconnection; column 10, lines 35-52; column 14, lines 10-14);
    - Asserting a reset signal (i.e. reset circuit; Figure 3-item 325; column 8, lines 28-38; column 9, lines 15-27) on a second interconnection controller in a second cluster (Figure 1-item 1721,1723) including a second plurality of processors in communication using a point-to-point architecture (i.e. point-to-point interconnection; column 14, lines 10-14).

However, the reference fails to show the establishing a link layer protocol on a connection between the first and second interconnection controllers. Nonetheless, this limitation would have been an obvious modification to the method as disclosed by Self, for one of ordinary skill in the art at the time of the invention, as further evidenced by Kelly.

In an analogous art, Kelly discloses clustered processing elements (abstract). Kelly further discloses establishing a link layer protocol on a connection between the

first an second interconnection controllers, (column 6, lines 20-42). One of ordinary skill in the art at the time of the invention would have been so motivated to accordingly modify the method of Self, so as to establish communications between network elements in the cluster with link and protocol with high bandwidth, (Kelly column 6, lines 21-22). However, the references fail to disclose polling for the presence of a second interconnection controller. Nonetheless, enabling and disabling polling was a well-known feature in the art, at the time of the invention, as further evidenced by Booth. Therefore, it would have been obvious for one of ordinary skill in the art to accordingly modify the features of Self and Kelly.

In an analogous art, Booth discloses polling for network link (abstract). Booth further discloses polling for a link to a second interconnection controller (column 20, line 55-column 21, line 6). One of ordinary skill in the art at the time of the invention, would be motivated to according modify the system of Self with enabled/disabled polling so as to provide link monitoring for establishing communication links, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40).

In reference to claims 13 and 24, Booth discloses wherein polling is performed continuously (column 20, line 55-column 21, line 6).

In reference to claims 14 and 25, Booth shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8).

In reference to claims 15 and 26, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim s 16 and 27, Self shows wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 17 and 28, Self shows wherein reinitialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 18 and 29, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claims 19 and 30, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

In reference to claims 20 and 31, Self shows wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 21, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 22, Self shows wherein the first interconnection controller includes, fence, reinitialization and cluster ID bits (column 11, lines 46-column 12, line 8; column 11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaShanya R. Nash whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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August 5, 2007

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